A triboelectric nanogenerator energy harvesting system based on load-aware control for input power from 2.4 μW to 15.6 μW

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ABSTRACT

This paper presents a triboelectric nanogenerator (TENG) energy harvesting system for ultra-low power applications. We propose a load-aware control algorithm to improve the power conversion efficiency as well as the voltage conversion efficiency. The control algorithm minimizes the conduction and switching losses within a switched capacitor charge pump (SCCP) by modulating its switching frequency based on the load condition. Furthermore, a hysteresis input regulation control was developed for preventing breakdown. The overall system was optimized by utilizing a compact spice model from the physical mechanisms of the employed TENG. The fabricated test chip in 65-nm process technology provides a regulated output voltage of 1.2 V with power conversion efficiency of 88% at 30 Hz excitation frequency when the TENG output voltage is 2.5 V.

1. Introduction

Recent development of various emerging systems such as implantable medical devices, wireless sensor nodes, and wearable electronics has opened a new era of applications such as Internet-of-Things (IoT) [1–6]. Self-sustainable, fully-integrated and low-cost power management is crucial in these applications. In this aspect, the use of energy harvesters as a primary energy source has been excessively studied to minimize the battery replacement/recharging cost and enhance the device lifetime [1–8].

Solar, thermal and mechanical energy harvesters have been used in many literatures as energy sources [5,8–13]. Among these energy sources, mechanical energy becomes promising due to its common existence in our daily life; it can be harvested from human, vehicles, and objects vibrations. In the last decades, the piezoelectric transducer has been widely used for energy harvesting despite its complex fabrication [1]. However, lately, TENG was introduced as a new promising mechanical energy harvester [13–18]. It generates electric power based on the coupling of triboelectrification and electrostatic induction as explained in Ref. [14,15]. The continuous variation of capacitance between two materials generates current flow and hence electric power. The fabricated TENG details along with its charge's generation procedure is discussed and detailed in Supplementary Fig. 1.

TENG becomes an attractive power source due to its fabrication simplicity, low cost, high flexibility, low weight, and small size [14]. Moreover, it can harvest energy from diverse vibration types in our daily life and can have various fabricated shapes (Supplementary Fig. 2), which makes it an adequate candidate for self-powered systems [14,15,19–22]. Excessive studies, since 2012, have been conducted in the material properties and instantaneous output power of the TENG device from the perspective of material-engineering [13]. However, design of efficient TENG energy harvesting circuits has not been comprehensively investigated. TENG characteristics including its high peak output voltage (Fig. 1) and limited output power needs to be carefully considered for designing efficient energy harvesting systems. These two barriers mainly stem from the high internal impedance (tens-hundreds of MQ) due to its capacitive nature. The first integrated TENG energy harvesting circuit was presented in Ref. [13]. It used the fractional open circuit maximum power point tracking (MPPT) technique and achieved a peak tracking efficiency of 97%. However, the MPPT control circuit consumes relatively large power and the harvested power is only 51.1% of the total input power. In addition, the input voltage to the energy harvesting circuit is 70 V, which cannot be adopted in mainstream semiconductor process technologies whose supply voltage is just a few

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In this work, the power conversion efficiency is calculated by dividing the interface circuit output power (regulated output power) by the interface circuit input power (TENG output DC power).

This work presents a novel TENG energy harvesting system assisted with a smart, efficient and low power load aware control technique for enhancing power conversion efficiency and voltage conversion efficiency. It reduces the switching and conduction losses in the implemented switched capacitor charge pump circuit. It shows a 36% improvement in power conversion efficiency when compared with [13]. Furthermore, hysteresis-based input regulation is proposed. This minimizes the power losses and the tracking efficiency degradation and prevents the proposed energy harvesting system from breakdown due to unacceptable high voltage.

The remainder of this paper is organized as follow. Section 2 explains the top architecture and the circuit implementation of the proposed TENG energy harvesting system as well as the proposed load aware control and input regulation techniques. Section 3 presents the measurement set-up and experimental results, followed by conclusions in section 4.
2. Proposed TENG energy harvesting system and circuit implementation

2.1. Electrical characteristics of TENG

Fig. 1(a) illustrates the operation of the employed TENG device based on the vertical contact mode. The top electrode consists of Perfluorooalkoxy alkane (PFA) and Aluminum [24]. PFA is a well-known material for excellent stability to strong chemicals and corrosion protection. These properties have been applied to TENGs [24]. The induced current flows when the TENG device is either pressed or released. Fig. 1(b) shows the output waveform ($V_{teng}$) of the employed TENG when it is stimulated by vertical vibrations. The peak output voltage levels depend on the pressure and the materials, while the frequency of the pulses follows the frequency of the vibrations (i.e. excitation frequency ($f_{ex}$)).

Unlike the piezoelectric transducers, $V_{teng}$ can have different positive and negative peak values. A dual-input bridge rectifier is reported in Ref. [13] to harvest positive ($V_{pos}$) and negative ($V_{neg}$) peaks separately. The rectified output voltage waveforms at no-load condition (TENG open-circuit characterization) as a function of the excitation frequency are shown in Supplementary Fig. 3. Fig. 1(c) depicts the relationship between the power and the TENG output voltage. The curves also show that at certain $f_{ex}$, an optimal voltage (i.e. $V_{mpp}$) exists where the output power is maximized. The power-voltage characterization curves shown in Fig. 1(c) suggest that, the $V_{mpp}$ varies with the excitation frequency, that depends, in the TENG case, determines the input power (Supplementary Fig. 3). The reason behind that is the variation of the TENG output impedance with the generated power (i.e. which depends on the excitation frequency). Hence, for efficient impedance matching, the $V_{mpp}$ variation with the excitation frequency is expected a depicted in Fig. 1(c). As shown in Fig. 1(c), $V_{mpp}$ exceeds 30 V when $f_{ex}$ is higher than 5 Hz. This requires high voltage process technology to regulate $V_{rect}$

Fig. 3. (a) Hysteresis-input regulation control and (b) timing diagram.
near $V_{\text{mpp}}$ as demonstrated in Ref. [13] using external voltage references due to the high voltage operation. However, this cannot be employed in mainstream process technologies where the supply voltage is just a few volt. Therefore, this work focuses on the operation region where the proposed TENG energy harvesting system can be directly employed as an on-chip power management solution. In this work, a conventional full-wave rectifier is employed as in Ref. [12, 23] since the rectified voltage ($V_{\text{rect}}$) is much less than $V_{\text{pos}}$ and $V_{\text{neg}}$ so that no high voltage process technology is necessary.

Utilizing the TENG output voltage characterization (Fig. 1 and Supplementary Fig. 3), a TENG spice model was developed to study its characterization and optimize the design of a power management circuit that can efficiently harvest the mechanical energy harvested from the newly proposed TENG. The developed model is detailed in Supplementary Fig. 4. The developed spice model results verify the accuracy of the proposed model and the validation of the deduced equations for $V_{\text{teng}}$ (Supplementary Fig. 5).

2.2. Proposed energy harvesting system architecture

Fig. 2 illustrates the proposed TENG energy harvesting system architecture. It scavenges mechanical energy and manages it to supply current ($I_{L}$) or store it in a super-capacitor ($I_{C}$). The proposed architecture comprises four main blocks, namely a 0.5 × power converter to step down $V_{\text{rect}}$, dynamic latched comparators with hysteresis-based input regulation control (HIRC) and load aware control (LAC), an excess energy storage circuit, and a digital core for supporting the LAC and HIRC schemes. First, upon the TENG vibration, the proposed HIRC regulates $V_{\text{rect}}$ around 2.5V preventing breakdown. Then, $V_{\text{rect}}$ is stepped down by the implemented SCCP to 1.2V supplying the IoT load. The losses within the SCCP are minimized using a proposed ultra-low power LAC circuit. It efficiently modulates the SCCP switching frequency according to the load condition (i.e. high, normal or light). Finally, using the HIRC output, the excess energy is stored using a supercapacitor, which can be used to supply the IoT load during the lack of input harvested energy.

2.3. Principle of hysteresis-based input regulation

As shown in Fig. 1, maximum power points ($V_{\text{mpp}}$) are formed at high voltage levels (e.g. > 30 V). However, mainstream process technologies prevent $V_{\text{rect}}$ from being close to $V_{\text{mpp}}$ due to the device reliability. Therefore, it limits the applications of the TENG energy harvesting systems. To address this, this work proposes an input regulation technique that regulates $V_{\text{rect}}$ within the maximum allowed voltage ($V_{\text{mpp-max}}$) of the employed technology. However, this requires a part of the harvested energy to be lost at various operating conditions (e.g. $f_{\text{sw}}$, $I_{L}$). The proposed hysteresis-based input regulation adopts an excess energy storage circuit that minimizes the harvested energy losses while maintaining the $V_{\text{rect}}$ regulation close to the maximum allowed voltage.

As shown in Fig. 3, the $V_{\text{rect}}$ level depends on the total output current ($I_T$) and the vibration frequency ($f_{\text{vib}}$) at steady state. $I_T$ is composed of two components, the load current ($I_L$) and the excess energy storage current ($I_C$). The flow rate of $I_L$ is controlled by the digital core along with the excess storage circuit. Thus, the main idea of the proposed input regulation technique is to regulate $V_{\text{rect}}$ near $V_{\text{mpp-max}}$ by modulating $I_L$ with respect to $I_C$ and $f_{\text{sw}}$.

Fig. 3 illustrates the simplified diagram of the proposed hysteresis-based input regulation. It consists of two comparators with two external references ($V_{\text{ref-high}}$ and $V_{\text{ref-low}}$), a 2-bit register, and a 5-bit counter. The comparator outputs ($\Phi_H$ and $\Phi_L$) are stored in the 2-bit register and fed to the 5-bit-counter. The counter output ($R_{\text{bits}}$) modulates $I_L$ by altering the resistance ($R$), which is implemented with a binary weighted resistor matrix. If $V_{\text{rect}}$ lies between $V_{\text{ref-high}}$ and $V_{\text{ref-low}}$, $R_M$ retains the value as well as $I_L$. The operation of the proposed input regulation scheme is controlled by $\Phi_H$ and $\Phi_L$ is summarized in Fig. 3(a). Fig. 3(b) shows the operation of the proposed input regulation scheme. At high $I_L$ and/or low $f_{\text{sw}}$, $V_{\text{rec-div}}$ goes below $V_{\text{ref-low}}$ (i.e. $\Phi_H = 1$, and $\Phi_L = 0$). The 5-bit counter output increments $R_{\text{bits}}$ for increasing $R_M$ and decreases $I_L$. $V_{\text{rect}}$ recovers and maintains its regulation around $V_{\text{mpp-max}}$. Similarly, at light $I_L$ and/or high $f_{\text{sw}}, V_{\text{rec-div}}$ goes above $V_{\text{ref-high}}$ (i.e. $\Phi_H = 0$, and $\Phi_L = 1$). Thus, the 5-bit counter decrements $R_{\text{bits}}$ so that $R_M$ decreases to compensate for the decrease of $I_L$. In both scenarios, the excess charges carried by $I_C$ are stored in a supercapacitor. These excess charges can be used to feed a second load or the charge pump circuit in case of low harvested energy. A part of the stored energy is lost in $R_M$ due to the limited voltage of the process technology while maintaining $V_{\text{rect}}$ near $V_{\text{mpp-max}}$.

2.4. Load-aware control algorithm

A switched capacitor charge pump (SCCP) with a gain of 0.5 is implemented to step-down $V_{\text{rect}}$. It is regulated at $V_{\text{mpp-max}}$ (~2.5 V) and

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Fig. 4. (a) Proposed load aware control flow-chart and (b) timing diagram.
Fig. 5. (a) Proposed TENG energy harvesting system test setup and (b) measured power conversion efficiency.

Fig. 6. (a) Proposed load aware control operation at $I_L$ variation and (b) hysteresis-based input regulation control across different $f_{ex}$ values.
provides a regulated output voltage (V_{out}) of ~1.2 V. However, the TENG output power is limited around V_{mpp-max} as shown in Fig. 1. Thus, it is critical to minimize the conduction and switching losses in the charge pump for improving power conversion efficiency as well as voltage conversion efficiency. Note that the power conversion efficiency is calculated by dividing the interface circuit output power (regulated output power) by the interface circuit input power (i.e. TENG output power). In general, voltage conversion ratio (i.e. 0.5) must be kept constant across various load conditions. However, it deviates from 0.5 when load current varies. To prevent the undesirable deviation in the voltage conversion ratio, the switching frequency (f_{sw}) of the charge pump must be controlled carefully depending on the load conditions. If f_{sw} is higher than the required one, it increases switching loss. Similarly, if f_{sw} is lower than the required one, it increases conduction loss. The proposed load aware control technique modulates the f_{sw} of the charge pump with I_{L} by monitoring the voltage conversion ratio.

As shown in Fig. 2, the proposed load aware control is implemented with a comparator and a 4-bit frequency divider. The comparator compares V_{rect-div} with V_{out-div}. V_{rect-div} and V_{out-div} are divided voltage levels of V_{rect} and V_{out} as indicated in Fig. 2. The comparator acts as a voltage conversion sensor, which indirectly reflects the I_{L} condition. The 4-bit frequency divider controls the ring oscillator (ROSC) output frequency by a 4-bit digital value ‘N’. ‘N’ is set by the comparator output (V_{comp}) to modulate f_{sw} with respect to I_{L} variations, maintaining the voltage conversion ratio around 0.5. Fig. 4 illustrates the flow chart of the proposed load aware control. It adopts an event/time driven technique for modulating f_{sw} across various load scenarios. Initially, ‘N’ is preset to an initial value by a power-on-reset (POR) block in Fig. 2. If V_{out} < 0.5V_{in} (i.e. V_{comp} = 0), f_{sw} is increased by decrementing ‘N’ by one bit. Likewise, if V_{out} > 0.5V_{in} (i.e. V_{comp} = 1), the 4-bit frequency divider increments ‘N’ by one bit after a defined time t_{d}, decreasing f_{sw}. For example, following the timing diagram depicted in Fig. 4, when I_{L} abruptly increases, V_{out} goes below 0.5V_{in} (i.e. V_{out-div} < V_{rect-div}). Thus, the proposed load aware control increases f_{sw} by decrementing ‘N’ by one bit at every detected V_{comp} negative edge for V_{out} recovery. Similarly, if V_{out} > 0.5V_{rect}, f_{sw} will be decreased by incrementing ‘N’ by one bit after a defined time ‘t_d’. At steady state, V_{out} oscillates around 0.5V_{rect}. Thus, by adjusting f_{sw} to a proper value with respect to the load conditions, the power conversion efficiency along with the voltage conversion efficiency can be increasingly improved.

3. Measurements results

The proposed TENG energy harvesting system was designed and fabricated in 65-nm CMOS process. Fig. 5(a) shows the test setup of the proposed TENG energy harvesting system and the comparison table. The test chip occupies a silicon area of 0.394 mm². A power amplifier is used to control the excitation frequency (f_{exc}) and the pressure of the vibrations applied on the fabricated TENG. These vibrations are generated by a commercial mini-shaker. It agitates one plate of the TENG while the other plate is fixed on a wall. A resistance matrix is used as R_{load} for characterization. The power conversion efficiency is recorded by calculating the power at V_{in} and V_{out} nodes (Fig. 5(b)) at each operating condition using current and voltage probes. Thus, the recorded power conversion efficiency (P_{out}/P_{in}) is improved by minimizing the energy losses within the power management circuit.

The slow TENG harvesting process (i.e. 100s of Sec) along with the big values of C_{min} and C_{out} (2 μF each) limits the bandwidth of the proposed control loops. Thus, the implemented dynamic latched comparators operate at a very low rate (~1 KHz) for ultra-low power consumption (~20 nW). Fig. 5(b) shows the power conversion efficiency at different f_{exc} when the output power of the proposed energy harvesting system changes. The test chip achieves a peak power conversion efficiency of 88% at f_{exc} = 30 Hz, which is achieved by the minimized conduction and switching losses in the charge pump through the proposed load aware control. Note that the compared work in Ref. [15] is using high voltage technology, which is not suitable for our target applications such as IoT and on-chip power management.

Fig. 6(a) demonstrates the operation of the proposed load aware control. When I_{L} increases, the comparator transmits pulses to the 4-bit frequencydivider in the digital core (Fig. 2) to modulate f_{sw} accordingly. f_{sw} increases one step at every V_{comp} negative pulse to restore V_{out} to its regulated value. This minimizes the conduction loss of the switched capacitor charge pump (SCCP) and maintains the voltage conversion ratio ~0.5. Thus, the proposed load aware control tracks the maximum power conversion efficiency after considering the load condition. The operation of the hysteresis-based input regulation is demonstrated in Fig. 6(b). In the proposed input regulation, two comparators outputs, \Phi_H and \Phi_L, monitor V_{rect} and maintain it between the two reference levels (V_{ref-high} and V_{ref-low}). They regulate it around V_{mpp-max} by modulating I_{L} flow rate, which is used to store the excess charges, as explained in section III. With the decrease of f_{exc} (i.e. 30 Hz→20 Hz), assuming constant I_{L}, V_{rect} goes below V_{ref-low}. Hence, \Phi_H turns to ‘0’, decreasing I_{L} and keeping V_{rect} above V_{ref-low}. Likewise, when f_{exc} increases from 20 Hz to 40 Hz, \Phi_L turns ‘1’, increasing I_{L}, maintaining V_{rect} below V_{ref-high}.

4. Conclusion

This work proposes a triboelectric energy harvesting system for ultra-low power applications such as IoT and wearable devices. Here, nominal supply voltage is a few volt. To make TENG an attractive energy source, high power conversion efficiency and low output voltage compatible to integrated circuits are substantial. To achieve these, this work proposes a load aware control technique for minimize the conduction and switching losses in the implemented switched capacitor charge pump, solving the limited harvested power issue. The proposed control technique successively achieves a maximum power conversion efficiency of 88% at f_{exc} 30 Hz, showing a 36% improvement compared with the prior art triboelectric energy harvesting system design in Ref. [15]. In addition, a hysteresis-based input regulation was developed to prevent the fabricated chip from breakdown, and store the excess harvested energy. The digital core complexity is implemented by using the digital integrated circuit design flow using hardware description language, which makes the proposed control techniques scalable.

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Karim Rawy: Conceptualization, Methodology, Validation, Writing - original draft. Ruchi Sharma: Investigation, Validation. Hong-Joon Yoon: Investigation, Formal analysis. Usman Khan: Investigation, Formal analysis. Sang-Woo Kim: Conceptualization, Supervision. Tony Tae-Hyoung Kim: Conceptualization, Supervision, Writing - review & editing.

Appendix A. Supplementary data

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References


Tony Tae-Hyoung Kim (M’06-SM’14) received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, Korea, in 1999 and 2001, respectively. He received the Ph.D. degree in electrical and computer engineering from University of Minnesota, Minneapolis, MN, USA in 2009. From 2001 to 2005, he worked for Samsung Electronics where he performed research on the design of high-speed SRAM memories, clock generators, and IO interface circuits. In 2007–2009 summer, he was with IBM T. J. Watson Research Center and Broadcom Corporation where he performed research on circuit reliability, low power SRAM, and battery backed memory design, respectively. On November 2009, he joined Nanyang Technological University where he is currently an associate professor. He received “Best Demo Award” at APC CAS2016, “Low Power Design Contest Award” at ISLPED2016, best paper awards at 2014 and 2011 ISOCC, “AMD/CICC Student Scholarship Award” at IEEE CICC2008, Departmental Research Fellowship from Univ. of Minnesota in 2008, “DAC/ISSCC Student Design Contest Award” in 2008, “Samsung Humantec Thesis Award” in 2008, 2001, and 1999, and “ETRI Journal Paper of the Year Award” in 2005. He is an author/co-author of over 130 journal and conference papers and has 17 US and Korean patents registered. His current research interests include low power and high performance digital, mixed-mode, and memory circuit design, ultra-low voltage circuits and systems design, variation and aging tolerant circuits and systems, and circuit techniques for 3D ICs. He is an IEEE senior member and served as the Chair of IEEE Solid-State Circuits Society Singapore Chapter. He serves as an Associate Editor of IEEE Transactions on VLSI Systems and has served numerous conferences as a committee member.